# Meeting Minutes 1 (Sunday 15/08/2021)

## Attendance

Hao Lin, Callum McDowell

### Time

11:10am to 2:40pm (3.5 hours)

## Goals

* Plan project timeline and assign roles.
* Complete first draft of FSM logic for pacemaker.

## Discussion

**Soft deadline for SCCharts and Nios: Wednesday 18th.**

**Work on report from Sat 21st onwards.**

#### Modes

* UART may be blocking - timing between modes differ, mode 2 slower? Should be okay, synchrony hypothesis.
* The mode switch is a 'mux' for input sources, and does not change the SCCharts FSM/logic.

#### Nios

* LED, interrupt and key (button) and switch interface
* UART communication with simulator
* Combine to switch modes.

Individual/extra work for Monday 16th. No group meeting required, but will potentially both be in 12:00-2:30pm?

#### FMS Design

It is okay to Slave AS to VS at defined time. No matter which S we are controlling from, the rate of pacing will be the same.

As VS is paced (i.e. signal VP) within the bounds URI >= t >= LRI, and AP is only generated (i.e. AS paced) if AEI elapses without AS, and AEI is a fixed period, then the rate at which VS is paced also governs the maximum rate at which AS may be paced.

This would only be a concern if timing were such that the VS was occurring faster than URI but an AS signal was not registered within the AEI. In this case an AP would be generated at a rate greater than URI, potentially enabling the faster heartbeat/occurrence of VS. Further research would have to be taken to determine if this is the correct approach, or if the pacemaker would benefit from also limiting the URI of AP.

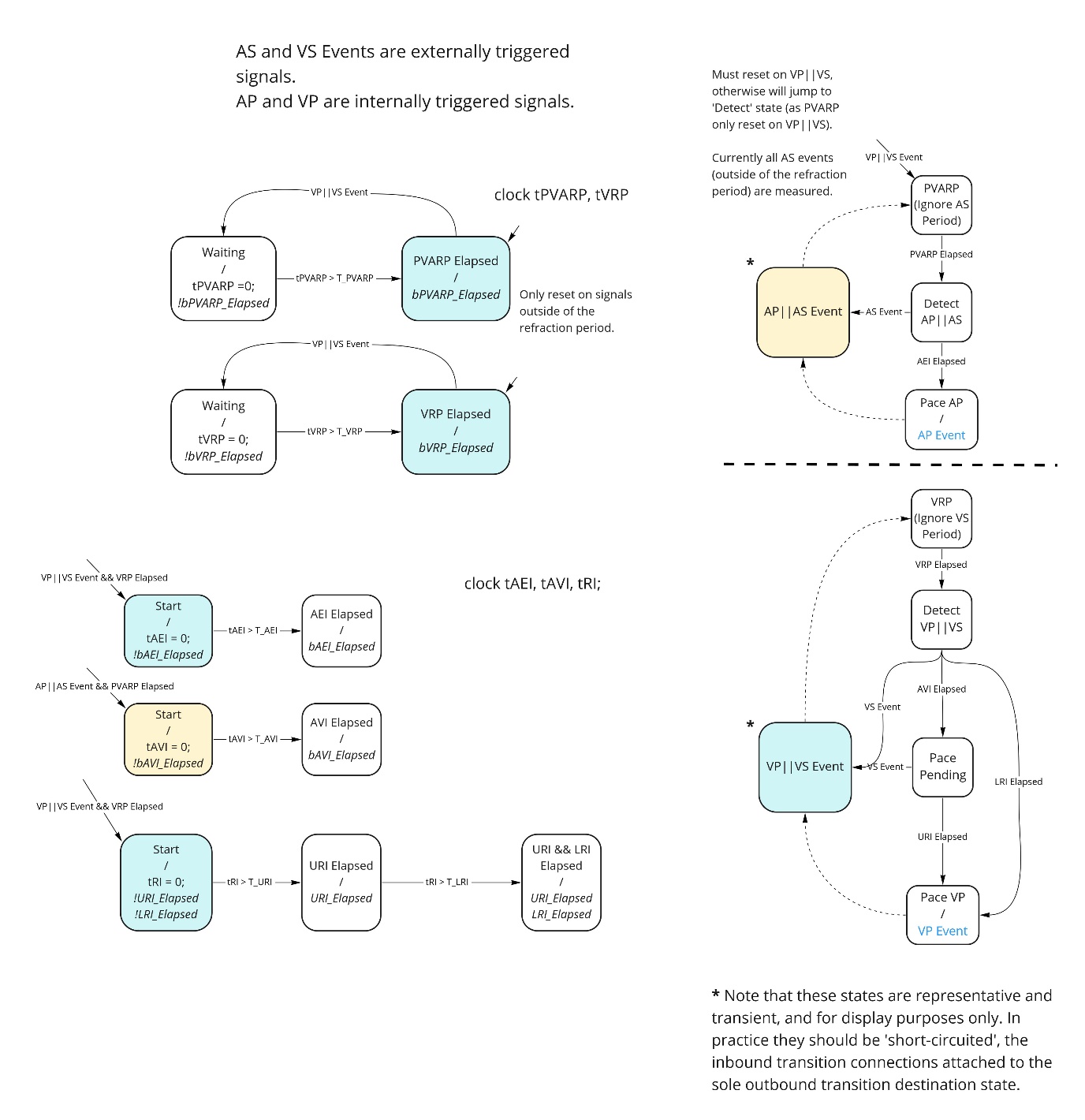
#### Failsafes

We can only assume timing intervals are set correctly because that is no internal method as to determine whether LRI or the URI value is correct. By design choice, we gave precedence to URI - pacemaker's intended operation rate.

Realistically, in industry these values should be safeguarded via logic and timing checks at compile and programming time

## Conclusion

First draft:



Concerns:

* This requires the ‘timer’ FSMs to be a child one-state FSM in parallel with the AP and VP pacemaker FSM, which may not be practical for SCCharts (which typically has a state in a larger FSM be comprised of regions with smaller FSMs).

## To Do

* Start work on Nios and hardware (@Callum)
* Code FSM into SCCharts (@Hao)
* Report (which can wait, but documentation as we go is priority)